THAT WHICH IS CLAIMED IS:

1. A bipolar junction transistor, comprising:

an intrinsic collector region of first conductivity type in a semiconductor substrate;

a trench in said substrate, adjacent said intrinsic collector region;

a base electrode of second conductivity type in said trench;

a base region of second conductivity type that is self-aligned to said base electrode and forms a P-N rectifying junction with said intrinsic collector region; and

an emitter region of first conductivity type that forms a P-N rectifying junction with said base region.

2. The transistor of Claim 1, further comprising a trench insulating layer disposed between said base electrode and a sidewall of said trench.

3. The transistor of Claim 2, wherein the sidewall of said trench defines an interface between said base region and said trench insulating layer.

4. The transistor of Claim 2, wherein said base region comprises:

an extrinsic base region of second conductivity type that is self-aligned to said base electrode, in said intrinsic collector region; and

an intrinsic base region of second conductivity type that is self-aligned to said base electrode and has a lower second conductivity type doping concentration therein relative to said extrinsic base region, in said intrinsic collector region.

5. The transistor of Claim 2, wherein said base electrode includes a base electrode extension that extends along a surface of said substrate; and wherein said emitter region is self-aligned to a sidewall of the base electrode extension.

6. The transistor of Claim 4, wherein said trench is ring-shaped; and wherein said extrinsic base region is ring-shaped.

7. The transistor of Claim 5, further comprising:

an electrically insulating sidewall spacer on the sidewall of the base electrode extension; and

an emitter electrode of first conductivity type on the surface of said substrate and on said electrically insulating sidewall spacer.

8. The transistor of Claim 7, further comprising a buried extrinsic collector region of first conductivity type in said substrate, said buried extrinsic collector region forming a non-rectifying junction with said intrinsic collector region.

9. The transistor of Claim 8, wherein an inner sidewall of said trench defines an intrinsic collector region mesa that extends between said buried extrinsic collector region and the surface of said substrate.

10. A method of forming a bipolar junction transistor, comprising the steps of:

forming a trench in a semiconductor substrate having an intrinsic collector region of first conductivity type therein;

forming a base electrode of second conductivity type in said trench;

forming a base region of second conductivity type that is self-aligned to said base electrode and forms a P-N rectifying junction with said intrinsic collector region; and

forming an emitter region of first conductivity type that forms a P-N rectifying junction with said base region.

11. The method of Claim 10, wherein said step of forming a trench is preceded by a step of forming an electrically insulating masking layer as a composite of a nitride layer and an oxide layer, on the semiconductor substrate; wherein said step of forming a trench comprises etching the semiconductor substrate, using the electrically insulating masking layer as an etching mask; wherein said step of forming a base electrode is preceded by a step of selectively etching the nitride layer to define a lateral recess within the electrically insulating masking layer; and wherein said step of forming a base electrode comprises depositing a layer of polysilicon of second conductivity type in the trench and in the lateral recess.

12. The method of Claim 11, wherein said step of forming a base region comprises diffusing dopants of second conductivity type from the base electrode into the intrinsic collector region to define an extrinsic base region therein.

13. The method of Claim 12, wherein the extrinsic base region is self-aligned to the lateral recess within the electrically insulating masking layer.

14. The method of Claim 12, wherein said step of forming an emitter region comprises the steps of:

etching the electrically insulating masking layer, using the base electrode as an etching mask;

forming an electrically insulating sidewall spacer on a sidewall of the base electrode;

forming a polysilicon emitter electrode of first conductivity type on the electrically insulating sidewall spacer; and

diffusing dopants of first conductivity type from the polysilicon emitter electrode into the intrinsic collector region.

15. The method of Claim 12, wherein said step of forming a base electrode is preceded by the step of lining a sidewall and a bottom of the trench with a trench oxide layer; and wherein the sidewall of the trench defines an interface between the trench oxide layer and the extrinsic base region.

16. The method of Claim 15, wherein said step of forming a trench comprises forming a ring-shaped trench in the semiconductor substrate; and wherein the bottom of the trench defines an interface between the intrinsic collector region and the trench oxide layer.

17. The method of Claim 14, wherein said step of forming an electrically insulating sidewall spacer on a sidewall of the base electrode is preceded by the step of implanting intrinsic base region dopants of second conductivity type into the intrinsic collector region, using the base electrode as an implant mask.

18. The method of Claim 17, wherein said step of forming a base electrode is preceded by the step of lining a sidewall and a bottom of the trench with a trench oxide layer; and wherein the sidewall of the trench defines an interface between the trench oxide layer and the extrinsic base region.

19. The method of Claim 18, wherein said step of forming a trench comprises forming a ring-shaped trench in the semiconductor substrate; and wherein the bottom of the trench defines an interface between the intrinsic collector region and the trench oxide layer.

20. The method of Claim 19, wherein the semiconductor substrate has a buried extrinsic collector region of first conductivity type therein; and wherein said step of forming a trench is preceded by the step of forming a collector contact region of first conductivity type in the substrate by implanting collector contact dopants of first conductivity type into the substrate and then diffusing the collector contact dopants.

21. A method of forming a bipolar junction transistor, comprising the steps of:

forming an electrically insulating layer on a surface of a semiconductor substrate having an intrinsic collector region of first conductivity type therein extending to the surface;

etching a lateral recess in the electrically insulating layer;

forming a polysilicon base electrode of second conductivity type in the lateral recess;

forming an extrinsic base region in the intrinsic collector region by diffusing dopants of second conductivity type from the polysilicon base electrode into the intrinsic collector region; and

forming an emitter region of first conductivity type in the intrinsic collector region.

22. The method of Claim 21, wherein the electrically insulating layer comprises a composite of a nitride insulating layer and an oxide insulating layer.

23. The method of Claim 21, wherein said step of etching a lateral recess in the electrically insulating layer is preceded by the step of etching a trench in the semiconductor substrate, using the electrically insulating layer as an etching mask; and wherein said step of forming a polysilicon base electrode in the lateral recess comprises forming a polysilicon base electrode in the trench.

24. The method of Claim 22, wherein said step of etching a lateral recess in the electrically insulating layer is preceded by the step of etching the electrically insulating layer to expose a sidewall thereon; and wherein said step of etching a lateral recess in the electrically insulating layer comprises selectively etching the nitride insulating layer using an etchant that etches the nitride insulating layer at a higher rate than the oxide insulating layer.

25. The method of Claim 24, wherein said step of forming an emitter region is preceded by the step of forming an intrinsic base region of second conductivity type that is self-aligned to the polysilicon base electrode, in the intrinsic collector region.

26. The method of Claim 25, wherein said step of forming an intrinsic base region comprises implanting dopants of second conductivity type into the intrinsic collector region, using the polysilicon base electrode as an implant mask.